Application Note

Application Note

AN1153

APM32F103xC Series Application Note

Version: V1.0

1 Introduction

This application note provides precautions to be taken when using the APM32F103xC series.

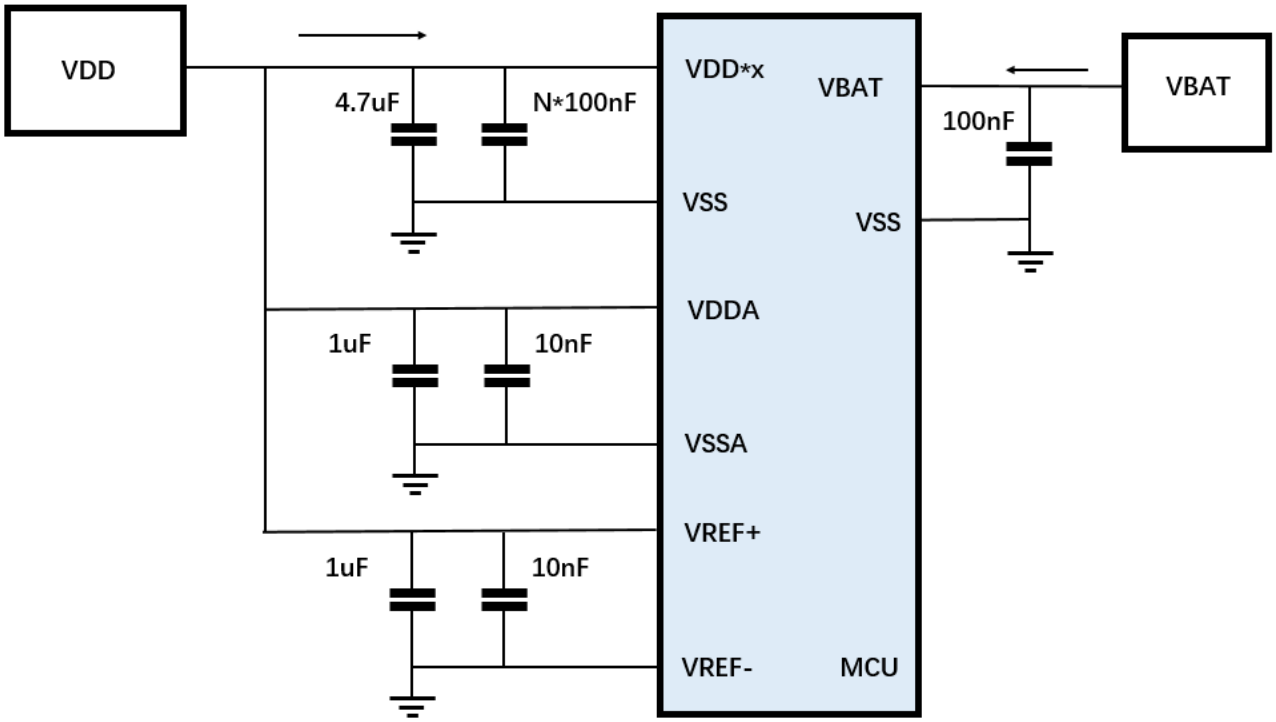
Contents

2 Note to Hardware Application Design

2.1 Design of MCU Filter Capacitor

The chip power ports (VDD, VSS) need to be connected in parallel to large and small filter capacitors. The effectiveness of capacitors depends on the optimal placement and connection type. PCB layout requires star-shaped wiring, and it is important to note that the external power supply passes through large and small capacitors and then connects to the chip. The large and small filter capacitors should be placed as close to the chip as possible within 4mm. The capacitor design reference is shown in Figure 1.

Figure 1 Capacitor Design



The VBAT pin can be connected to an external battery (1.8V<3.6V). If there is no external battery, an external 100nF ceramic capacitor should be connected to the VDD power supply together.

VDD must be connected to VDD power supply of an external capacitor (N 100nF ceramic capacitor(s) and a tantalum capacitor not less than 4.7μF). VDD*x represents that the number of VDD is x.

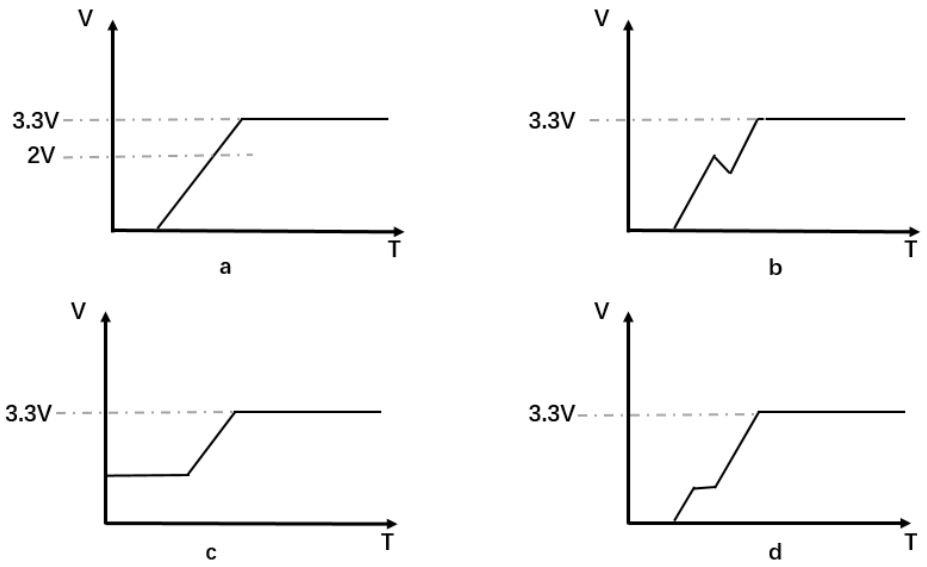
VDDA is connected to VDD, and supplies power to ADC, reset module, RC oscillator and PLL analog part. When ADC is used, VDDA is greater than or equal ato 2.4V. VDDA and VSSA must be connected to VDD and VSS respectively.

The VREF+ pin can be directly connected to VDDA or an external reference voltage can be used separately. The voltage range of VREF+ must be between 2.4V and VDDA.

2.2 Precautions for MCU Power Supply Ramp Rate

The MCU's power supply ramp rate should meet the required maximum and minimum value limits, namely greater than 0.5V/min and less than 100V/ms respectively. The power on/down time from 0V to 3V requires at least 30us. Too high or too low power-on rate may cause the MCU to fail to work normally; MCU needs to be powered down to below 300mV before being powered on again, and the above time must meet the requirements within the full temperature range. The power-on startup waveform needs to meet the waveform a in Figure 2, while the other three waveforms are incorrect.

Figure 2 Power-on Waveform



2.3 The peripheral module uses VDD and VSS

When MCU is used to control the power supply or power-on process of external modules, too high power-on rate should be avoided to prevent the problem of VDD voltage being pulled down due to sudden current changes. To ensure stable operation of the system and protect the circuit from potential damage, it is recommended to adopt appropriate delay measures for steady power supply conversion.

Appropriate buffer elements such as capacitors and resistors can be added to the MCU power supply end to buffer the fast power-on and power-down speed of the power supply, so that voltage dip will not be caused to VDD due to instantaneous high current demand. If sudden dip is caused for this reason, the drop speed must also meet the requirements of the MCU's power supply ramp rate. In the scenarios shown in Figures 3 and 4, in order to avoid power fluctuation, connect a buffer circuit (composed of MOS transistor, capacitor, and resistor) in series on the control circuit, or connect a 10R resistor in series and a capacitor of 10uF and above on the circuit, to form a fast power-on/power drop protection circuit. If the capacitance is large enough,

the power down will be slow and the power-down magnitude can be very small.

Figure 3 Power Supply of IO Control Peripheral Module

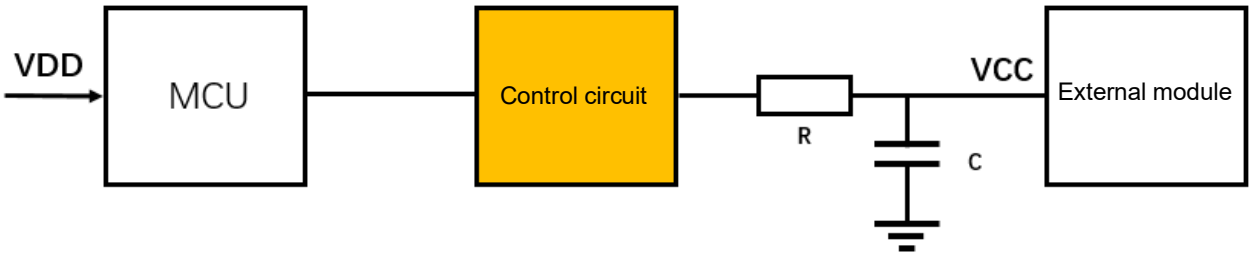
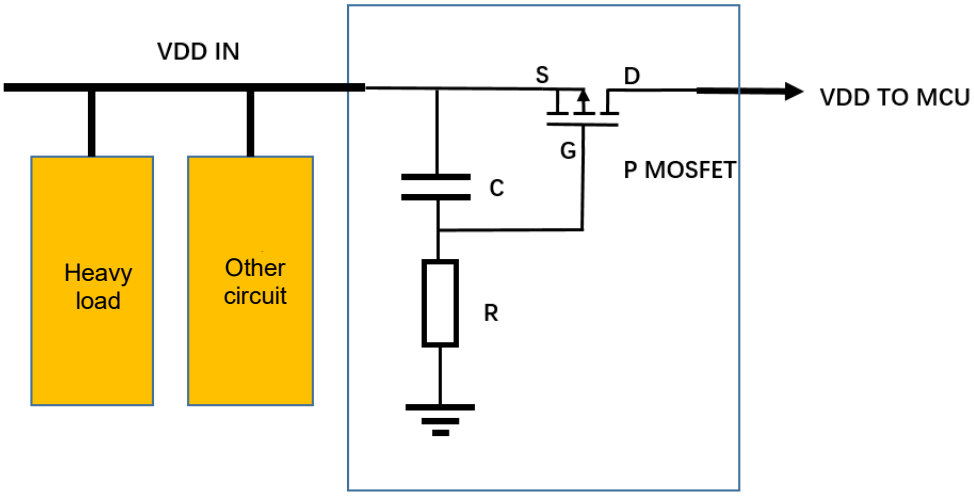


Figure 4 Shared Power Supply for Peripherals



2.4 External and High-frequency Signals

Attention should be paid to checking whether an instantaneous increase in load may be caused by zero-crossing signals, relay signals, AC loads, etc. The load impact can be mitigated by bypass capacitors.

For high-frequency IIC clock lines, high-frequency SPI clock lines, etc., it is important to check whether instantaneous peak currents will be generated.

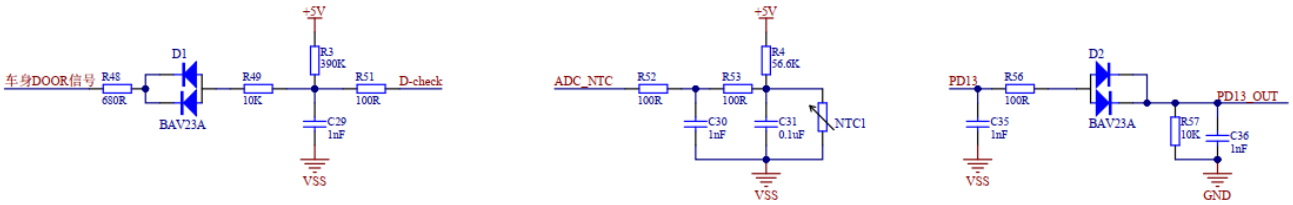
2.5 Connect the Input/Output signal port to a current limiting resistor in series and connect the capacitor to VSS in parallel

For Input/Output ports (e.g. ADC, external interrupts, communication interfaces, etc.), it is recommended to connect to the protective resistors in series in circuit design. The resistance value should be considered and calculated, and the theoretical maximum current should not

exceed the limit parameters that the chip port can withstand; the resistors connected in series and capacitors connected in parallel should be placed as close as possible to the chip pins, and the resistors should be connected in series before the capacitors are connected in parallel. The ground of the filter capacitor of the peripheral module must be connected to the ground that has passed through the large and small filter capacitors (VDD, VSS). As shown in Figure 5, the IO port is connected in series to a 100R resistor and connected in parallel to a 1nF capacitor.

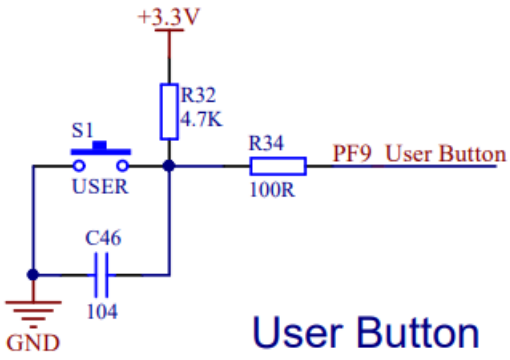
Note that in the design of PCB interconnection (similar to separating lamps from control modules, separating sensors from control modules), this series-connected resistors and parallel-connected capacitors should be placed on the PCB board of the chip. Reasonable parameters and placement positions can effectively prevent damage to the chip ports by ESD/EOS.

Figure 5 An Example of Resistor and Capacitor Connection



For button circuits, the recommendations are as follows:

Figure 6 Button Circuit



As shown in Figure 6, connect a small resistor R34 in series, e.g. 100R, in the GPIO, and place the capacitor C46 as close as possible to the button S1 when designing the PCB So that it can avoid the negative impact pressure generated by buttons.

2.6 IO voltage cannot be higher than VDD voltage

When the IC is not powered by VDD, but there is voltage at the IO port, this voltage will be supplied to the IC through a pull-up protection diode. Or when the IC is powered by VDD, but there is a higher voltage at the IO port than VDD, the voltage difference between this voltage and VDD will cause the pull-up protection diode to conduct, making the current flow into VDD. Under normal circumstances, IO cannot exceed 0.3V above VDD.

This phenomenon can easily cause the following hazards:

(1) Too high current will cause the clamp diode on the IO port to quickly overload and be damaged.

(2) It will make MCU reset unsuccessfully.

(3) It will cause disorder in the chip program.

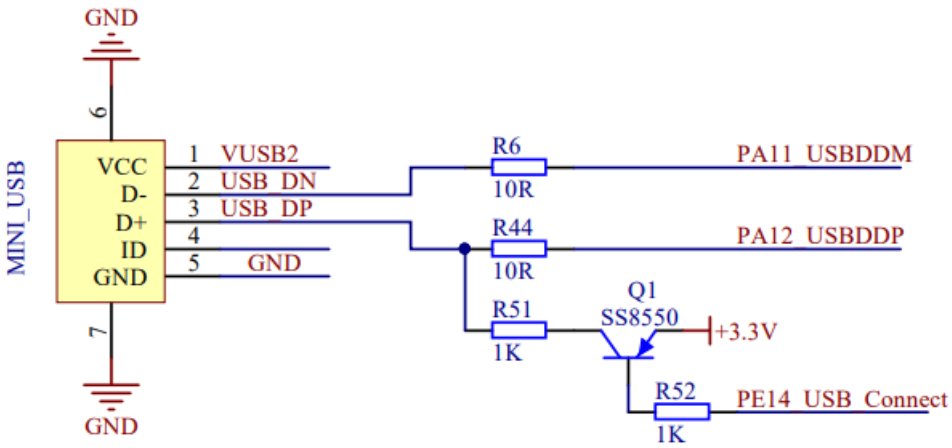
(4) A latch-up effect will result.

2.7 Pay Attention to Protection for Exposed Ports

For communication ports, ESD protection measures are required. A small resistor (e.g. 10R, 100R) can be connected in series on the signal line to limit the amplitude of ESD current; transient voltage suppressor diodes (TVS) can be connected in parallel on the signal line, near the interface position. It is as shown in Figure 7 Communication Circuit.

There is a hot-plugging risk in the burning port, and it should be protected by first contacting GND and then contacting IO during the connection.

Figure 7 Communication Circuit



3 Precautions for Software Application

3.1 Precautions for GPIO Operation

1. Unused GPIO ports should be set to output low level or connect an external 100Ω resistor for pull-down.

2. Different GPIO pins should avoid being configured with the same multiplexing function.

3. When the chip VDD is powered on within the range of 0V-2V, the GPIO port is in an uncertain state, and attention should be paid to the impact of unstable condition of GPIO on the stability of the post-stage drive circuit; when VDD is powered on above 2V, after the chip completes the power-on reset, the status of the GPIO port will be executed according to the program settings.

4. When the GPIO port is configured as a multiplexing push-pull output, it is necessary to connect an external pull-up resistor; when it is configured as a floating input, it is necessary to connect an external pull-up resistor or modify the software to a pull-up input, otherwise the voltage may be affected by external factors and stable levels cannot be outputted or read.

3.2 AC characteristics of PA8 and PC8

PA8 and PC8 are equipped with an external 50pF load capacitor. At 2V low voltage, the output rate is 10MHz square wave, and the output duty cycle is high, ranging from 60% to 70%.

It is recommended to avoid the simultaneous occurrence of low-voltage and low-speed (2V, 10MHz) conditions when this pin is used. The I/O speed is related to the configuration, normal at high speed and abnormal at low speed. For example, if I/O is configured to 50MHz mode and outputs 10M at 2V, the duty cycle is normal.

3.3 HSE startup time

When the timeout value of the software that sets the HSE startup time is too small (e.g. 0x0500), external clock startup ready timeout may occur, which may result in the failure of using HSE as the clock source.

To ensure normal startup of the crystal oscillator, it is recommended to modify the external clock wait time timeout value to at least 0x3200. The specific operation is modifying the macro definition of HSE_STARTUP_TIMEOUT.

3.4 USART3 and FSMC Remapping

USART3 remapping PD8 and PD9 pins conflicts with FSMC clock. Specifically: when remapping PD8 and PD9 as serial pins, enable FSMC clock but the serial communication cannot be used normally.

Choose either of the following solutions:

Use partial remapping function of USART3 (PC10 and PC11) or default configuration (PB10 and PB11).

When USART3_TX is remapped to PD8 as a serial port pin, disable the SMC function.

3.5 Precautions for obtaining accurate RTC calibration clock output from PC13

RTC can output the internal RTC second pulses, alarm signals, and calibration clocks to the outside through the PC13 pin. The output pulses can be selected by configuring the BAKPR_CLKCAL register.

When LSECLK is used as the clock source for RTC, and the ready flag bit of the external low-speed clock is set to 1, configure the PC13 to output the calibration clock signal after delay for a period of time, or wait for a period of time before measuring the calibration signal. It is important to note that the waiting time may vary with the parameters, temperature, and voltage differences of the crystal oscillator. The recommended delay reference time is 1s.

3.6 USBD and CAN can be used simultaneously

USBD1 and CAN2 can be used simultaneously, USBD2 and CAN1 can be used simultaneously, USBD1 and USBD2 cannot be used simultaneously, and CAN1 and CAN2 can be used simultaneously. Although there are actually two identical USBD pins, they cannot be used simultaneously, which means that there is only one. Users can achieve "simultaneous use" through remapping (multiplexing function of pins).

Use according to the recommendations of Datasheet and User Manual.

3.7 Precautions for CAN2_IO Remapping

If CAN2 uses remapping pins (e.g., I/O initialization) and then performs other peripheral remapping operation, CAN2 will fail to remap. It is required to perform CAN2 remapping (e.g., I/O initialization) operation after all peripheral remapping operations.

3.8 Module timing of SPI

When SPI (SPI_cmd() function ENABLE) is enabled, after SPI parameters are modified, the timing transmission of SPI for one byte is 16 clocks (normally 8 clocks).

The recommended initialization standard operation of SPI is specifically:

Initialize the corresponding SCK MOSI, MISO and NSS, and enable SPI. To modify the parameters, first enable SPI (SPI_cmd() function DISABLE) and then modify the corresponding configuration.

3.9 Precautions for PWR Sleep Mode

The first execution of the WFE instruction is invalid, and the second WFE instruction can work properly. The reason for this problem is the difference in M3 kernel version.

3.10 Precautions for FPU Function

The larger the input value of FPU is, the higher the probability of occurrence of errors is.

Suggest controlling the FPU input value within ±3π. It is important to note that the operation acceleration effect of FPU only applies to the functions in the LIB library, and it has no significant acceleration effect on other operations such as +, -, ×, ÷, and matrix permutation.

3.11 Precautions for Low-power Wake-up

The low-power and AHB frequency division scenario may result in abnormal clearing of the dcode buffer, thus entering hardfault.

The recommended operations for low-power wake-up scenarios of WFI and WFE are as follows:

For the WFI low-power wake-up scenarios, AHB should not divide the frequency (i.e. ensure that the first interrupt vector data is read and returned from Flash, rather than returned from buf). After the low power is awakened, enter the interrupt service function, first read an address from each Flash bank in the interrupt service function and then start to execute the real user program.

For the WFI low-power wake-up scenarios, AHB should not divide the frequency (i.e. ensure that the first interrupt vector data is read and returned from Flash, rather than returned from buf). After the low power is awakened, start sequential execution, first read an address from each bank and then start to execute the real user program.

3.12 Precautions for Flash Erase

For the interrupt scenarios, before erasing Flash, shield the interrupt, there will be no scenarios of entering the interrupt in the erasing process, and it will change to the regular erase scenario.

For conventional erase scenarios (sequential program execution), after initiating the erase, before executing FlASH_GetBank1Status, add: while (FLASH->SR&FLASH_FLAG_BANK1_BSY)==FLASH_FLAG_BSY; and AHB remains frequency not divided.

3.13 Pin interrupt configuration

Repeatedly configuring interrupts for the same pin may lead to false triggering of pin interrupts.

Do not repeatedly configure interrupts for the same pin; after the interrupt function is used, shield this interrupt before it can be initialized again.

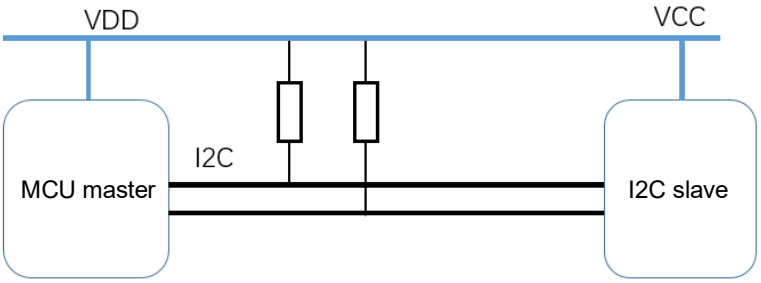
3.14 Precautions for I2C

In the process of sudden power failure and recovery of pull-up power supply of SCL/SDA, there is a possibility that the combination of SCL/SDA voltage and logic timing may trigger START but not STOP, resulting in the bus remaining in BUSY state. Recommended avoidance scheme:

1. The pull-up power supply of I2C must be stable to prevent the power supply from dropping too low due to instability during use. For common scenarios of I2C master-slave communication, the following hardware design is recommended:

a. The host and slave share power supply;

Figure 8 I2C Communication Circuit



b. When the host and slave cannot share power supply, it is recommended to connect the power supply of pull-up resistor to the power supply of host MCU.

2. The bus can also be released by resetting the slave. If EEPROM is used as a slave, it is impossible to reset the salve using the software, and the bus release function needs to be added to the I2C host when establishing a new communication. Due to the probability of bus locking, the bus BUSY status timeout function can be added. Combination of the two can improve the robustness of the system.

3. If the I2C device on the bus can recognize power failure, turn off the I2C module before power failure.

4 Revision history

Table 1 Document Revision History

Date	Version	Revision History
March,2025	1.0	New

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